

Enroll No

K.E.Society's
Rajarambapu Institute of Technology, Rajaramnagar
(An Empowered Autonomous Institute, affiliated to SUK)
Unit Test -II (2025-26)

Q.P. Code
UT 3109

S.Y. B.Tech.-Electronics & Telecommunication Engineering
Course Code: EC2014 **Course Name: Digital Design**

Day & Date: Thursday, 18/09/2025

Time: 3.45pm to 4.45pm

Max Marks- 25

- Instructions:**
- 1) All questions are compulsory.
 - 2) Figures in rounded () brackets within the question, indicate the scheme of marking for respective part of the question, whereas, figures in the first right column indicate total marks for that whole question.
 - 3) CO is the index number of the Course Outcome statement.
 - 4) The Bloom's taxonomy level (BL) for 1,2,3,4,5 and 6 is remember, understand, apply, analyze, evaluate and create respectively.
 - 5) Assume suitable data if necessary.
 - 6) Use of non-programmable calculators is allowed

			Marks	BT Level	COs
Q.1	A	Explain (3M), with a logic schematic (1M), the operation of a full subtractor.	4	L2	3
	B	Design a BCD adder that adds two BCD digits and produces a BCD sum digit.	8	L4	2
Q.2	A	Draw (1M) a 4:1 multiplexer using basic logic gates and describe (4M) its operation with an example.	5	L1	1
	B	Design a 8:3 encoder using basic logic gates. OR Design a BCD-to-7-segment decoder that displays '1' on a common-cathode 7-segment display.	8	L4	2

